

Claims

That which is claimed:

1. A method of forming a nonvolatile memory device, comprising:
forming a first oxide layer on a substrate;
5 forming a nitride layer on the first oxide layer;
forming a second oxide layer on the nitride layer;
patterning the second oxide layer so as to expose the nitride layer;
forming a first polysilicon layer on the second oxide layer and the exposed
portion of the nitride layer;
10 etching the first polysilicon layer and the nitride layer so as to expose the
second oxide layer and the first oxide layer and to form polysilicon spacers on the
nitride layer;
etching the polysilicon spacers so as to expose portions of the nitride layer, the
exposed portions of the nitride layer comprising charge trapping layers;
15 etching the exposed portion of the first oxide layer to expose a portion of the
substrate;
forming a third oxide layer on the exposed portion of the substrate, the
exposed portions of the nitride layer, and the second oxide layer;
forming a second polysilicon layer on the third oxide layer; and
20 planarizing the second polysilicon layer so as to expose the second oxide layer,
the second polysilicon layer comprising a gate electrode that overlaps portions of the
charge trapping layers, the third oxide layer comprising a gate insulating layer.
2. The method of Claim 1, further comprising:
25 etching the exposed portion of the second oxide layer, the nitride layer, and the
first oxide layer using the gate electrode as a mask so as to expose the substrate.
3. The method of Claim 2, further comprising:
forming a source region and a drain region in exposed portions of the substrate
30 on adjacent sides of the gate electrode.
4. The method of Claim 3, wherein forming the source region and the
drain region comprises:

forming the source region and the drain region in exposed portions of the substrate on adjacent sides of the gate electrode using ion implantation.

5. The method of Claim 3, further comprising:

5 etching a middle portion of the gate electrode and the gate insulating layer so as to expose the substrate and form first and second gate electrodes and first and second gate insulating layers; and

forming an impurity region in the exposed portion of the substrate between the first and second gate electrodes and the first and second gate insulating layers.

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6. The method of Claim 5, wherein forming the impurity region in the exposed portion of the substrate between the first and second gate electrodes and the first and second gate insulating layers comprises:

15 forming the impurity region in the exposed portion of the substrate between the first and second gate electrodes and the first and second gate insulating layers using ion implantation.

7. The method of Claim 1, wherein forming the first oxide layer on the substrate comprises:

20 forming the first oxide layer on the substrate using thermal oxidation.

8. The method of Claim 1, wherein forming the nitride layer on the first oxide layer comprises:

25 forming the nitride layer using low-pressure chemical vapor deposition on the first oxide layer.

9. The method of Claim 1, wherein forming the second oxide layer on the nitride layer comprises:

30 forming the second oxide layer using low-pressure chemical vapor deposition on the nitride layer.

10. The method of Claim 1, wherein etching the first polysilicon layer comprises:

etching the first polysilicon layer using an isotropic etch back process.

11. The method of Claim 1, wherein etching the exposed portion of the first oxide layer comprises:

5 etching the exposed portion of the first oxide layer using a wet etching process.

12. The method of Claim 1, wherein forming the third oxide layer on the exposed portion of the substrate, the exposed portions of the nitride layer, and the
10 second oxide layer comprises:

forming the third oxide layer on the exposed portion of the substrate, the exposed portions of the nitride layer, and the second oxide layer using chemical vapor deposition.

13. The method of Claim 1, wherein forming the second polysilicon layer on the third oxide layer comprises:

forming the second polysilicon layer on the third oxide layer using chemical vapor deposition.

14. The method of Claim 1, wherein planarizing the second polysilicon layer comprises:

planarizing the second polysilicon layer using chemical mechanical polishing.

15 A method of fabricating a nonvolatile memory device, comprising:
25 forming a vertical structure in which a first oxide layer pattern, a nitride layer pattern, and a second oxide layer pattern are sequentially stacked on a semiconductor substrate, wherein part of the surface of the semiconductor substrate is exposed by the vertical structure, and the surface of the nitride layer pattern is exposed by the second oxide layer pattern;

30 forming a third oxide layer on exposed surfaces of the vertical structure and the semiconductor substrate;

forming a polysilicon layer on the third oxide layer;

forming a control gate electrode of the polysilicon layer pattern by performing

a planarization process until the second oxide layer pattern is exposed;

performing an etching process using the control gate electrode as an etching mask until part of the surface of the semiconductor substrate is exposed, wherein an ONO layer where a tunneling layer of the first oxide layer pattern, a charge trapping layer of the nitride layer pattern and a blocking layer of the third oxide layer are sequentially stacked to be aligned with a gate insulating layer is arranged; and forming a source region and a drain region by performing an ion implantation process on the semiconductor substrate exposed by the control gate electrode.

10 16. The method of Claim 15, wherein the forming of the vertical structure further comprises:

forming a first oxide layer, a nitride layer, and a second oxide layer sequentially on the semiconductor substrate;

forming a second oxide layer pattern exposing part of the surface of the nitride layer by patterning the second oxide layer;

forming an inter-layer on the exposed surface of the nitride layer and the second nitride layer pattern;

forming a spacer on sides of the second oxide layer pattern by isotropically etching the inter-layer;

20 forming a nitride layer pattern exposing part of the surface of the first oxide layer by etching the nitride layer using the second oxide layer pattern and the spacer as etching masks;

exposing a part of the nitride layer pattern by removing the spacer;

forming the first oxide layer pattern by etching the first oxide layer using the nitride layer pattern as an etching mask; and

forming the third oxide layer on an exposed surface of the semiconductor substrate, an exposed surface of the nitride layer pattern, and the second oxide layer pattern.

30 17. The method of Claim 16, wherein the inter-layer is a polysilicon layer.

18. The method of Claim 16, wherein isotropic etching of the inter-layer is performed by etch-back method.

19. The method of Claim 16, wherein etching of the first oxide layer is performed by a wet etching method.

5 20. The method of Claim 15, wherein the third oxide layer is formed by chemical vapor deposition.

21. The method of Claim 20, further comprising thickening the third oxide layer by performing thermal oxidation after performing chemical vapor deposition.
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22. The method of Claim 15, wherein the planarization process is performed by a chemical mechanical polishing method.

23. A method of fabricating a nonvolatile memory device comprising:
15 forming a pair of spaced vertical structures in which each vertical structure has a structure of a first oxide layer pattern, a nitride layer pattern and a second oxide layer pattern sequentially stacked on a semiconductor substrate, wherein part of the surface of the semiconductor substrate is exposed by the vertical structures, and part of the surface of the nitride layer pattern is exposed by the second oxide layer pattern;
20 forming a third oxide layer on the exposed surfaces of the vertical structures and the semiconductor substrate;
 forming a polysilicon layer by performing a planarization process until the second oxide layer pattern is exposed;
 performing an etching process using the control gate electrode as an etching
25 mask until part of the surface of the semiconductor substrate is exposed, wherein a pair of separate ONO layers and the third oxide layer is arranged, wherein each ONO layer has a structure of a tunneling layer of the first oxide layer pattern, a charge trapping layer of the nitride layer pattern, and a blocking layer of the third oxide layer sequentially stacked;
30 forming a mask layer pattern, which exposes part of the surface of the polysilicon layer pattern, on the polysilicon layer pattern;
 forming a first control gate electrode and a second control gate electrode which are composed of the polysilicon layer pattern and arranged to be spaced apart from

one another, and a first gate insulating layer and a second gate insulating layer which are formed of the third oxide layer and arranged under the lower portion of the first control gate electrode and the second control gate electrode; and

5 forming a source region, a drain region and impurity area by performing ion implantation on the semiconductor substrate exposed by the first control gate electrode and the second control gate electrode, wherein the source region is formed on the semiconductor substrate adjacent to the charge trapping layer of the lower portion of the first control gate electrode, the drain region is formed on the semiconductor substrate adjacent to the charge trapping layer of the lower portion of
10 the second control gate electrode, and the impurity region is formed on the semiconductor substrate between the first control gate electrode and the second control gate electrode.

24. The method of Claim 23, wherein the forming of the pair of vertical
15 structures further comprises:

forming sequentially a first oxide layer, a nitride layer, and a second oxide layer on the semiconductor substrate;

forming a pair of second oxide layer patterns exposing a middle portion of the surface of the nitride layer by patterning the second oxide layer;

20 forming an inter-layer on the exposed surface of the nitride layer and the second oxide layer pattern;

forming spacer on the sides of the second oxide layer pattern by isotropically etching the inter-layer;

25 forming a pair of nitride layer patterns exposing a middle portion of the surface of the first oxide layer by etching the nitride oxide using the second oxide layer patterns and the spacer as etching masks;

exposing a portion of the nitride layer patterns by removing the spacer;

30 forming a first oxide layer pattern exposing a middle portion of the surface of the semiconductor substrate by etching the first oxide layer using the nitride patterns as an etching mask; and

forming a third oxide layer on an exposed surface of the semiconductor substrate, an exposed surface of the nitride layer patterns, and the second oxide layer patterns.

25. The method of Claim 24, wherein the inter-layer is a polysilicon layer.

26. The method of Claim 25, wherein isotropic etching of the inter-layer is
5 performed by etch-back method.

27. The method of Claim 24, wherein etching of the first oxide layer is
performed by a wet etching method.

10 28. The method of Claim 23, wherein the third oxide layer is formed by
chemical vapor deposition.

29. The method of Claim 28, further comprising thickening the third oxide
layer by performing thermal oxidation after performing chemical vapor deposition.
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30. The method of Claim 23, wherein the planarization process is
performed by a chemical mechanical polishing method.

31. A method of forming a non-volatile memory device, comprising:
20 forming an oxide/nitride/oxide structure on a substrate, wherein a portion of
the substrate is exposed between portions of the oxide/nitride/oxide structure, the
oxide/nitride/oxide structure comprising a first oxide layer on the substrate, a nitride
layer on the first oxide layer, and a second oxide layer on the nitride layer opposite the
substrate, wherein portions of the nitride layer adjacent the exposed portion of the
25 substrate are free of the second oxide layer;

forming a third oxide layer on the second oxide layer, on the exposed portions
of the nitride layer, and on the exposed portion of the substrate;

forming a conductive layer on the third oxide layer;

planarizing the conductive layer to expose oxide of the second oxide layer
30 and/or third oxide layer; and

after planarizing the conductive electrode, removing remaining portions of the
third oxide layer, the second oxide layer, the nitride layer, and the first oxide layer
exposed by the planarized conductive electrode.

32. A method of forming a non-volatile memory device, comprising:
forming a first oxide layer on a substrate;
forming a nitride layer on the first oxide layer;
5 forming a second oxide layer on the nitride layer wherein a portion of the
nitride layer is exposed between portions of the second oxide layer;
forming spacers on exposed portions of the nitride layer adjacent the second
oxide layer so that a portion of the nitride layer remains exposed between the spacers;
removing portions of the nitride layer and the first oxide layer exposed by the
10 spacers to thereby expose portions of the substrate between the spacers;
removing the spacers;
forming a third oxide layer on the exposed portion of the substrate, on exposed
portions of the nitride layer adjacent the second oxide layer, and on the second oxide
layer;
15 forming a conductive electrode on the third oxide layer between the portions
of the second oxide layer.

33. A method according to Claim 32 wherein forming the conductive
electrode comprises:
20 forming a conductive layer on the third oxide layer between portions of the
second oxide layer and opposite the second oxide layer; and
planarizing the conductive layer to expose oxide of the second oxide layer
and/or third oxide layer.

- 25 34. A method according to Claim 33, further comprising:
after planarizing the conductive electrode, removing remaining portions of the
third oxide layer, the second oxide layer, the nitride layer, and the first oxide layer
exposed by the planarized conductive electrode.